TRANSMITTAL OF APPEAL BRIEF

Docket No.
SON-2274

In re Application of: Mamoru Kudo

Application No.	Filing Date	Examiner	Group Art Unit
10/000,347-Conf. #9724	December 4, 2001	G. Patel	2655

Invention: PHASE LOCKED LOOP CIRCUIT FOR REPRODUCING A CHANNEL CLOCK (AS AMENDED)

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed: June 18, 2004 .

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Dated: June 18, 2004

Ronald P. Kananen
Attorney Reg. No. : 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750

Docket No.: SON-2274
(80001-2274)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Mamoru Kudo

Application No.: 10/000,347 | Confirmation No.: 9724

Filed: December 4, 2001 | Art Unit: 2655

For: PHASE LOCKED LOOP CIRCUIT FOR REPRODUCING A CHANNEL CLOCK (as amended) | Examiner: G. Patel

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal Brief under Rule 192 appealing the final decision of the Examiner dated December 23, 2003. Each of the topics required by Rule 192 is presented herewith and is labeled appropriately.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Invention
VI. Issues

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 012519, frame 0128.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Total Number of Claims in Application.

- There are 4 claims pending in this application.

Current Status of Claims

- Claims canceled: 1-2
- Claims withdrawn from consideration but not canceled: none
- Claims pending: 5
- Claims allowed: none
- Claims rejected: 3-7

Claims On Appeal

- The claims on appeal are claims 3-7.

IV. STATUS OF AMENDMENTS

No amendment Subsequent to the final rejection of December 23, 2003.

V. SUMMARY OF INVENTION

The present invention relates to a phase-locked loop circuit for reproducing a channel clock in synchronism with data read from a disk-shaped recording medium driven for rotation, and is particularly suitable for playback of a plurality of kinds of disk-shaped recording media in different recorded data formats.

In PLL circuits for reproducing a channel clock in synchronism with data read from a disk-shaped recording medium driven for rotation, the frequency dividing ratio of frequency dividers provided in desired signal paths is made changeable according to the reproduced signal format of a CD reproduced signal or a DVD reproduced signal, for example. Although the frequency of the channel clock in synchronism with the reproduced signal differs in different signal formats, the above configuration makes it possible to reproduce the channel clock properly in accordance with a plurality of signal formats only by the operation of changing the frequency dividing ratio in a PLL circuit.

The digital PLL processing unit 5 has a three-stage PLL circuit system including a system PLL circuit 5A, an HIF-PLL circuit 5B, and a digital PLL circuit 48 (figure 2). The HIF-PLL circuit 5B includes a channel clock generation reference signal frequency divider **42**, a switching frequency divider **43**, and a phase comparator **44** (figure 4).

The channel clock generation reference signal frequency divider **42** divides a channel clock generation reference signal **Vclk** (specification as originally filed at page 20, lines 2-4).

The switching frequency divider **43** has a switch **SW21** (figure 4 of specification as originally filed), a first switching frequency divider **43a** and a second switching frequency

divider **43b** (specification as originally filed at page 27, lines 8-12 and figure 4). The first and second switching frequency dividers **43a and 43b** receive a high-frequency signal **HIF** (figure 4 of the specification as originally filed). The first switching frequency divider **43a** divide the high-frequency signal **HIF** by a first dividing ratio (1/98) to generate a first divided signal (figure 4 of the specification as originally filed). The second switching frequency divider **43b** divide the high-frequency signal by a second dividing ratio (1/558) to generate a second divided signal (figure 4 of the specification as originally filed). The switch **SW21** outputs the first divided signal during playback of a first recording medium and outputs the second divided signal during playback of a second recording medium (page 27, line 20 to page 28, line 6).

The phase comparator **44** receives the divided channel clock generation reference signal and one of the first and second divided signals (page 27, lines 18-20), and compares the phase of the divided channel clock generation reference signal with one of the first and second divided signals to output a phase error signal (page 20, lines 18-24).

VI. ISSUES

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 3-7 under 35 U.S.C. 112, first paragraph.

Whether the Examiner erred in rejecting claims 3-7 under 35 U.S.C. 112, second paragraph.

These issues will be discussed hereinbelow.

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, claims 3-7 stand or fall together.

In Section VIII below, Applicant has included arguments supporting the separate patentability of the claim group as required by M.P.E.P. § 1206.

VIII. ARGUMENTS

In the Final Office Action of December 23, 2003:

The Examiner rejected claims 3-7 under 35 U.S.C. 112, first paragraph.

The Examiner rejected claims 3-7 under 35 U.S.C. 112, first paragraph.

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

General Matters

M.P.E.P. 707.07(f) states that "the importance of answering such arguments is illustrated by *In re Herrmann*, 261 F.2d 598, 120 USPQ 182 (CCPA 1958) where the applicant urged that the subject matter claimed produced new and useful results. The court noted that since applicant's statement of advantages was not questioned by the examiner or the Board of Appeals, it was constrained to accept the statement at face value and therefore found certain claims to be allowable. See also *In re Soni*, 54 F.3d 746, 751, 34 USPQ2d 1684, 1688 (Fed Cir. 1995) (Office failed to rebut applicant's argument)."

The Examiner rejected claims 3-7 under 35 U.S.C. 112, first paragraph.

The Final Office Action contends that page 17, line 6, of the specification as originally filed defines signal HIF as a high-frequency signal. The Final Office Action further contends that HIF only goes to one divider (figure 2, unit 43), however claim 3 claims the signal HIF going to two frequency dividers (first and second). The Final Office Action additionally contends that a phase comparator which receives a reference signal and one of first and second signals is also not defined because first of all NONE of the frequency signals are going directly to any one of the phase comparators (41 or 44). The Final Office Action finally contends that the first and second divide signals cannot be generated as claimed.

In response, claim 3 and the claims dependent thereon include the features of:

a channel clock generation reference signal frequency divider that divides a channel clock generation reference signal;

a switching frequency divider having a switch, a first switching frequency divider and a second switching frequency divider,

said first and second switching frequency dividers receiving a high-frequency signal,

said first switching frequency divider dividing said high-frequency signal by a first dividing ratio to generate a first divided signal,

said second switching frequency divider dividing said high-frequency signal by a second dividing ratio to generate a second divided signal,

said switch outputting said first divided signal during playback of a first recording medium and outputting said second divided signal during playback of a second recording medium; and

a phase comparator, said phase comparator receiving said divided channel clock generation reference signal and one of said first and second divided signals,

said phase comparator compares the phase of said divided channel clock generation reference signal with one of said first and second divided signals to output a phase error signal.

The first paragraph of 35 U.S.C. §112 "requires only an objective enablement; the invention needs to be sufficiently disclosed through illustrative examples or terminology to teach those of ordinary skill in the art how to make and how to use the invention as broadly as it is claimed" (emphasis added). *Musco Corp. v. Qualite Inc.*, 41 USPQ2d 1954 (Fed. Cir. 1997). See also M.P.E.P §§2164.01, 2164.04.

"The purpose of the 'written description' requirement is broader than to merely explain how to 'make and use'; the applicant must also convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention. The invention is, for purposes of the 'written description' inquiry, whatever is now claimed." *Vas-Cath Inc. v. Mahurkar*, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). See also M.P.E.P. §2163.02. "The applicant does not have to utilize any particular form of disclosure to describe the subject matter claimed." *In re Alton*, 37 USPQ2d 1578, 1581 (Fed. Cir. 1996).

In addition, "for claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims." *General Electric Co. v. Nintendo Co.*, 50 USPQ2d 1910, 1914 (Fed. Cir. 1999).

As shown at least within figures 2, 4 and other figures and descriptions throughout the specification, claim 3 and the claims dependent thereon include the features of:

a channel clock generation reference signal frequency divider **42** that divides a channel clock generation reference signal **Vclk** (specification as originally filed at page 20, lines 2-4);

a switching frequency divider **43** having a switch **SW21** (figure 4 of specification as originally filed), a first switching frequency divider **43a** and a second switching frequency divider **43b** (specification as originally filed at page 27, lines 8-12 and figure 4),

said first and second switching frequency dividers **43a and 43b** receiving a high-frequency signal **HIF** (figure 4 of the specification as originally filed),

said first switching frequency divider **43a** dividing said high-frequency signal **HIF** by a first dividing ratio (1/98) to generate a first divided signal (figure 4 of the specification as originally filed),

said second switching frequency divider **43b** dividing said high-frequency signal by a second dividing ratio (1/558) to generate a second divided signal (figure 4 of the specification as originally filed),

said switch **SW21** outputting said first divided signal during playback of a first recording medium and outputting said second divided signal during playback of a second recording medium (page 27, line 20 to page 28, line 6); and

a phase comparator **44**, said phase comparator **44** receiving said divided channel clock generation reference signal and one of said first and second divided signals (page 27, lines 18-20),

said phase comparator **44** compares the phase of said divided channel clock generation reference signal with one of said first and second divided signals to output a phase error signal (page 20, lines 18-24).

Thus, the claims contain subject matter that was described within the specification in such a way to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

The Examiner rejected claims 3-7 under 35 U.S.C. 112, second paragraph.

This rejection is traversed at least for the following reasons.

The Final Office Action contends that within claim 3, lines 3-4, "a channel clock generation reference signal frequency divider that divides a channel clock generation reference signal" is unclear and confusing. The Final Office Action further contends that it is not clear which divider the Applicants are claiming, also selecting either one of leads to even more confusion because none of them defines what is happening down the claim, when it comes feeding the signal in phase comparator [there are also two phase comparators]. The Final Office Action finally contends that HIF only goes to one dividers (unit 43) not both of them.

In response, claim 3 and the claims dependent thereon include the features of:

a channel clock generation reference signal frequency divider **42** that divides a channel clock generation reference signal **Vclk** (specification as originally filed at page 20, lines 2-4);

a switching frequency divider **43** having a switch **SW21** (figure 4 of specification as originally filed), a first switching frequency divider **43a** and a second switching frequency divider **43b** (specification as originally filed at page 27, lines 8-12 and figure 4),

said first and second switching frequency dividers **43a and 43b** receiving a high-frequency signal **HIF** (figure 4 of the specification as originally filed),

said first switching frequency divider **43a** dividing said high-frequency signal **HIF** by a first dividing ratio (1/98) to generate a first divided signal (figure 4 of the specification as originally filed),

said second switching frequency divider **43b** dividing said high-frequency signal by a second dividing ratio (1/558) to generate a second divided signal (figure 4 of the specification as originally filed),

said switch **SW21** outputting said first divided signal during playback of a first recording medium and outputting said second divided signal during playback of a second recording medium (page 27, line 20 to page 28, line 6); and

a phase comparator **44**, said phase comparator **44** receiving said divided channel clock generation reference signal and one of said first and second divided signals (page 27, lines 18-20),

said phase comparator **44** compares the phase of said divided channel clock generation reference signal with one of said first and second divided signals to output a phase error signal (page 20, lines 18-24).

The language found within the claims particularly point out and distinctly claim the subject matter that Applicant regards as the invention.

Conclusion

No prior art has been cited against these claims. Thus, all claims are deemed allowable as a result. Withdrawal of the rejections and allowance of the claims is respectfully requested.

IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: June 18, 2004

Respectfully submitted,

By_____
Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750
Attorney for Applicant

APPENDIX A

3. A phase-locked loop circuit for reproducing a channel clock, said phase-locked loop circuit comprising:

a channel clock generation reference signal frequency divider that divides a channel clock generation reference signal;

a switching frequency divider having a switch, a first switching frequency divider and a second switching frequency divider,

said first and second switching frequency dividers receiving a high-frequency signal,

said first switching frequency divider dividing said high-frequency signal by a first dividing ratio to generate a first divided signal,

said second switching frequency divider dividing said high-frequency signal by a second dividing ratio to generate a second divided signal,

said switch outputting said first divided signal during playback of a first recording medium and outputting said second divided signal during playback of a second recording medium; and

a phase comparator, said phase comparator receiving said divided channel clock generation reference signal and one of said first and second divided signals,

said phase comparator compares the phase of said divided channel clock generation reference signal with one of said first and second divided signals to output a phase error signal.

4. A phase-locked loop circuit as claimed in claim 3, further comprising:

a low-pass filter, said low-pass filter generating a low-frequency signal having a level corresponding to said phase error signal;

a voltage controlled oscillator outputting a frequency signal, the oscillation frequency of said frequency signal being controlled by the level of said low-frequency signal; and

a high-frequency signal frequency divider generating said high-frequency signal from dividing said frequency signal by a variable,

said variable being changed such that said high-frequency signal is at a first frequency during said playback of said first recording medium and is at a second frequency during said playback of said second recording medium.

5. A phase-locked loop circuit as claimed in claim 3, wherein said channel clock is in synchronism with data read from a disk-shaped recording medium driven for rotation.

6. A phase-locked loop circuit as claimed in claim 3, wherein said first recording medium has a standard different than that of said second recording medium.

7. A phase-locked loop circuit as claimed in claim 3, wherein said first recording medium is a first disk-shaped recording medium and said second recording medium is a second disk-shaped recording medium.